REMARKS

Claims 24, 27, and 33 have been canceled without prejudice. Claims 1, 13, 16, 18, 21, 25, 26, 29-31, and 34 have been amended. Claims 35 and 36 have been added. Accordingly, claims 1-23, 25, 26, 28-32, and 34-36 are currently pending in this application.

The subject matter of canceled claims 24, 27, and 33 is now contained in claims 1, 25, and 31, respectively.

Claims 1-4, 7-11, and 13-34 stand rejected under 35 U.S.C. §102 as being anticipated by Nair et al., US Patent No. 6,366,320 ("Nair"). This rejection is respectfully traversed.

Nair relates to a semiconductor circuit having an analog storage array and a sense amplifier array. According to Nair the circuit also includes an analog multiplexer through which a differential signal pair is driven into a signal processing pipe. Nair at abstract. Nair fails to disclose all of the elements of any of claims 1-4, 7-11, 13-23, 25, 26, 28-32, and 33.

The present invention relates, in part, to an image sensor apparatus. Accordingly, amended independent claim 1 recites an apparatus comprising, *inter alia*, "groups of image sensors, each group comprising subgroups of sensors; subgroup select circuits, each of which is coupled to an output from a respective subgroup of sensors." Amended independent claim 1 further recites "a first bus for each group coupled to the outputs of the associated subgroup select circuits" and "a first isolation circuit coupled to each first bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage."

Amended independent claim 31 recites "an imager device" comprising, *inter alia*, "groups of image sensors, each group comprising a plurality of columns of an image

sensor array" and "a plurality of group select circuits, each of which is coupled via a first bus to outputs from the column select circuits associated with a respective one of the groups." Amended independent claim 31 further recites "a first isolation circuit coupled to each first bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage."

Similarly, amended independent claim 34 recites "an imager device" comprising, *inter alia*, "an array of image sensors organized into supergroups comprising groups of subgroups of image sensors;" "group select circuits, each of which is coupled to outputs of subgroup select circuits associated with a respective one of the groups;" and "at least two group buses, each group bus coupled to outputs of the subgroup select circuits associated with a respective group. Amended independent claim 34 further recites "a first isolation circuit coupled to each group bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage."

The present invention also relates, in part, to a method of operating an image sensor. Accordingly, amended independent claim 25 recites a method comprising, *inter alia*, "selectively isolating from said readout circuit the groups of pixels not associated with the selectively enabled group select circuit by disabling the subgroup select circuits and group select circuits not associated with the selectively enabled group select circuit and applying a predetermined voltage to at least one first bus coupled to the disabled group select circuits by operating a switch coupled to the at least one first bus."

Nair, however, is silent about an isolation circuit comprising a switch for selectively connecting a bus of the analog multiplexer 118 to a predetermined voltage. Therefore, Nair fails to disclose such an isolation circuit connected as recited by amended independent claims 1, 31, and 34; or the act of isolating as recited by amended independent claim 25. The Examiner cited gate pairs in Nair's analog multiplexers 180-

186 as isolation circuits. Office Action at 3. The gate pairs, however, do not selectively connect a bus of the analog multiplexers 180-186 to a predetermined voltage. Instead, the gate pairs provide a pathway for a signal from the storage array through the analog multiplexer 118.

Amended independent claims 16 and 19 also recite methods. As amended, independent claim 16 recites a method comprising, *inter alia*, "selectively enabling a group select circuit to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits" and, "when the group select circuit is enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the group select circuit to the charge mode read-out amplifier."

Similarly, amended independent claim 19 recites a method comprising, *inter alia*, "selectively enabling a supergroup select circuit from a set of supergroup select circuits and a series-connected group select circuit from an associated set of group select circuits to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits" and, "when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the series-connected group select circuit and supergroup select circuit to the charge mode read-out amplifier."

Nair fails to disclose "when the group select circuit is enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the group select circuit to the charge mode read-out amplifier," as recited by amended independent claim 16. Likewise, Nair fails to disclose that "when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential

manner," as recited by amended independent claim 19; or "selectively enabling a group select circuit and a subgroup select circuit to allow sequential readout of un-amplified pixel signals from each sensor in said subgroup to a readout circuit," as recited by amended independent claim 25. Instead, Nair teaches that signals from the storage cells of the storage array 110 are fed into a sense amplifier array 114 prior to entering the analog multiplexer 118 and the signal processing pipe 126. Nair at col. 3, line 13 to col. 4, line 22. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 5, 6, and 12 stand Claims 1-4, 7-11, and 13-34 stand rejected under 35 U.S.C. §103 as being unpatentable over Nair. This rejection is respectfully traversed.

As discussed above, Nair fails to disclose all the elements of amended independent claim from which claims 5, 6, and 12 depend. Accordingly, for at least the reasons discussed above with respect to independent claim 1, withdrawal of this rejection is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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